

Quadrics Compliance & Performance test record

Test

Location	Quadrics, Bristol, UK	Date	8th October 2004
Tested by	Daniel Blueman		

System under test

Vendor	hp	System	DL585
Processor	2.2Ghz Quad Opteron	Chipset	AMD 8131 rev 12
BIOS	A01 (08/02/2004)	OS	hp Linux for HPC (RH EL 3)
Configuration as tested: 2GB DDR333 memory over 2 NUMA nodes. Only processors 0 & 1 installed.			

Quadrics equipment

Product	QsNetII QM500B	Part No.	3X-CM500-BA rev A02
Device driver	4.24qsnet	Toolchain	gcc-3.2.2-4, binutils-2.12.90.0.15-74
qsnet2libs	1.8.3-0	qsnetmpi	1.24-40

Basic compliance

Mechanical fit	No issues
BAR settings	All PCI-X BAR regions setup correctly
MTRR settings	All MTRRs setup as expected
PCI-X bridge/tunnel settings	Max Outstanding Split Read Requests should be initialised to a value of 3, rather than 1 for full performance
Device driver	No compatibility issues observed

Base PCI-X performance

Max DMA read b/w	880.18 MB/s
Max DMA write b/w	933.16 MB/s
Max PIO write b/w	476.65 MB/s
128 byte PIO write b/w	476.55 MB/s
round-trip base latency	1.24 uS

Application performance

Test setup	1x DL585 and 1x DL145 nodes, each through with 10m cable and single switch stage.
MPI half round trip latency	2.01 uS (2.48 uS [*])
Put half round trip latency	1.18 uS (1.35 uS [*])
MPI peak unidirectional BW	874.86 MB/s @ 1 MB (874.86 MB/s @ 1 MB [*])
Peak bi-directional BW	846.63 MB/s @ 1 MB (834.92 MB/s @ 1 MB [*])

Reliability/Soak testing

Description	(not performed)
Data transferred	
Errors logged	

Comments

All tests executed after Max Outstanding Split Read Requests PCI-X register on elan4 increased from value 1 to 3 with:

```
# setpci -d 14fc:1 7a.b=0x22
```

[*] Predicted measurements, calculated from:

$$\text{result} = \text{val}(\text{DL585toDL145}) * 2 - \text{val}(\text{DL145toDL145})$$