

Quadrics Compliance & Performance test record

Test

Location	Dalco, Switzerland	Date	19/07/2006
Tester	Daniel J Blueman <daniel.blueman@quadrics.com>		

System under test

Vendor	Dalco	System	DALC0 Server r2164i
Processor	Intel DC Woodcrest 3.0GHz, 1066/1333MHz FSB, 4MB shared L2 cache	Chipset	Intel 5000X
BIOS	R45	OS	RedHat EL AS 4 update 3, 2.6.9-34.EL.qp2.0smp
Configuration as tested	8GB DDR2 FBDIMM memory @ 633/667MHz		

Quadrics equipment

Product	QsNet II Elan4 rev B	Part no.	QM500-BB
Device driver	5.22.1qsnet	Toolchain	gcc-3.2.2-54, binutils-2.12.90.0.15-124
qsnet2libs	qsnet2libs-2.2.9-0	qsnetmpi	qsnetmpi-1.24-47.intel81

Basic compliance

Mechanical fit	No problems
BAR settings	Correct
PAT/MTRR settings	PAT is in use and working as expected
PCI-X bridge settings	optimal: 12 MOST, 512 MMRBC
Device driver	No warnings or unexpected messages

Base PCI-X performance

read latency	0.60 us
round-trip base latency	1.09 us
DMA read b/w	894.78 MB/s
DMA write b/w	918.39 MB/s
PIO write b/w (128)	814.87 MB/s
PIO write b/w (max)	814.87 MB/s

Application performance

Test setup	32-way switch with 2m cables
MPI half round trip latency	1.62 us
Put half round trip latency	1.12 us
MPI peak unidirectional b/w	877.54 MB/s at 4 MB message size
Peak bi-directional b/w	881.19 MB/s at 4 MB message size

Comments

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Reliability/soak testing (if applicable)

Description
Data transferred
Errors logged